REMARKS

The amendment to Paragraph 30 of the specification describes aspects of FIG. 3 and does not add new matter. New claims 29-30 and 32-33 are supported by FIG. 3 and the amendment to Paragraph 30.

New claims 31 and 34 are embodied in the buried oxide layer (BOX) 335 shown in FIG. 7 and described in Paragraph 37 of the specification.

The Examiner indicated that claims 23-28 are allowed. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner rejected claims 1-16 under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicant's admitted prior art, as disclosed in figures 1-2 and their description in the instant application in view of Bohr (U.S. Patent No. 6,617,681).

Applicants respectfully traverse the §103(a) rejections with the following arguments.

35 U.S.C. §103(a)

The Examiner rejected claims 1-16 under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicant's admitted prior art, as disclosed in figures 1-2 and their description in the instant application in view of Bohr (U.S. Patent No. 6,617,681).

Claims 1-10

Since Applicant has canceled claims 2, 5, and 8-10, the rejection of claims 2, 5, and 8-10 is moot.

Applicant respectfully contends that claim 1 is not unpatentable over Applicant's admitted prior art in view of Bohr, at least because Applicant's admitted prior art in view of Bohr does not teach or suggest the particular feature: "An integrated circuit, comprising: ... a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit".

The Examiner argues: "Applicant's admitted prior art fails to disclose a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit. However, Bohr discloses a backside I/O pad (224) electrically connected to a backside via of an integrated circuit structure (see figure 15)."

As first example why Applicant's admitted prior art in view of Bohr does not teach or suggest the preceding particular feature of claim 1, Applicant's admitted prior art in view of Bohr does not teach or suggest "An integrated circuit, comprising: ... a backside I/O pad". The integrated circuit chip 100 of FIGS. 1 and 2 of Applicant's admitted prior art does not disclose a backside I/O pad. FIG. 15 of Bohr does not disclose an integrated circuit comprising a backside I/O pad; i.e., the backside via in FIG. 15 is not disclosed by Bohr as being comprised by an

integrated circuit. Thus, the Examiner has not cited any prior art that discloses "An integrated circuit, comprising: ... a backside I/O pad" as required by claim 1.

As second example why Applicant's admitted prior art in view of Bohr does not teach or suggest the preceding particular feature of claim 1, Applicant's admitted prior art in view of Bohr does not teach or suggest "a backside via of the integrated circuit". The integrated circuit chip 100 of FIGS. 1 and 2 of Applicant's admitted prior art does not disclose a backside via. FIG. 15 of Bohr does not disclose an integrated circuit comprising a backside via; i.e., the backside I/O pad 224 in FIG. 15 is not disclosed by Bohr as being comprised by an integrated circuit. Thus, the Examiner has not cited any prior art that discloses "a backside via of the integrated circuit" as required by claim 1.

Furthermore, Applicant respectfully contends that the Examiner's argument for modifying Applicant's admitted prior art with the alleged teaching of Bohr is not persuasive. The Examiner argues that "it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die to a substrate (column 12, lines 35-37)."

In response, Applicant contends that FIG. 1 of Applicant's admitted prior art discloses front-side solder balls 155 which are adapted to electrically and mechanically couple the integrated circuit chip 100 to a substrate (such as to a chip carrier or circuit board as is well known in the art). The Examiner has not disclosed any motivation in the prior art for coupling the integrated circuit chip 100 to a substrate at the backside of the integrated circuit chip 100.

Thus, it is not obvious to incur extra structural complexity, additional fabrication steps, and additional cost to add a capability that already is available to the integrated circuit chip 100 of FIG. 1 of Applicant's admitted prior art.

Moreover, Applicant's admitted prior art teaches away from use of a backside via to connect the pins 175 in FIG. 1 of Applicant's admitted prior art to a substrate through a backside via. See specification, Paragraph 6, which recites: "There is no wiring in portions of M1 level 120 and M2 level 125 contained within redistribution portion 170. A plurality of core I/O pins 175 are located in redistribution portion 170 at M3 level 130". In other words, FIG. 1 shows that a backside via or other conductive wiring would have to located in the redistribution portion 170 in order for the I/O pins 175 to be connected to a substrate through the backside of the integrated circuit chip 100. However, the preceding quote from the specification teaches away from placing such conductive wiring in the redistribution portion 170.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Bohr, and that claim 1 is in condition for allowance. Since claims 3-4 and 6-7 depend from claim 1, Applicants contend that claims 3-4 and 6-7 are likewise in condition for allowance.

In addition with respect to claim 3, Applicant disagrees with the Examiner's allegation that "Applicant's admitted prior art discloses I/O pins (175) formed in a lowest interconnect level of an integrated circuit chip." Applicants note that in FIG. of Applicant's specification, the I/O pins 175 are formed in the M3 interconnect level which is not a lowest interconnect level of the integrated circuit chip 100. The interconnect level M2 is lower than interconnect level M1, and the interconnect level M4 is higher than interconnect level M2. In contrast, FIG. 3 of Applicant's

specification shows the I/O pins 275 of the present invention formed in the M1 interconnect level, which is indeed a lowest interconnect level of the integrated circuit chip 200.

In addition with respect to claim 7, Applicant disagrees with the Examiner's allegation that Applicant's admitted prior art discloses "additional I/O pins in metallization layer (130)", since the only I/O pins disclosed in FIG. 1 and the specification are the I/O pins 175 identified by the Examiner in relation to claim 1.

In addition with respect to claim 10, Applicant disagrees with the Examiner's allegation that Applicant's admitted prior art discloses "additional predefined circuitry having a plurality of I/O pins contained in metallization layer (140)", since the only I/O pins disclosed in FIG. 1 and the specification are the I/O pins 175 identified by the Examiner in relation to claim 1.

Claims 11-16

Since Applicant has canceled claims 13-14, the rejection of claims 13-14 is moot.

Applicant respectfully contends that claim 11 is not unpatentable over Applicant's admitted prior art in view of Bohr, at least because Applicant's admitted prior art in view of Bohr does not teach or suggest the particular feature: "connecting a backside I/O pad of the integrated circuit electrically to each I/O pin through a backside via of the integrated circuit".

The Examiner argues: "Applicant's admitted prior art fails to disclose a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit. However, Bohr discloses a backside I/O pad (224) electrically connected to a backside via of an integrated circuit structure (see figure 15)."

As first example why Applicant's admitted prior art in view of Bohr does not teach or

suggest the preceding particular feature of claim 11, Applicant's admitted prior art in view of Bohr does not teach or suggest "a backside I/O pad of the integrated circuit". The integrated circuit chip 100 of FIGS. 1 and 2 of Applicant's admitted prior art does not disclose a backside I/O pad. FIG. 15 of Bohr does not disclose an integrated circuit comprising a backside I/O pad; i.e., the backside I/O pad 224 in FIG. 15 is not disclosed by Bohr as being comprised by an integrated circuit. Thus, the Examiner has not cited any prior art that discloses "a backside I/O pad of the integrated circuit " as required by claim 11.

As second example why Applicant's admitted prior art in view of Bohr does not teach or suggest the preceding particular feature of claim 11, Applicant's admitted prior art in view of Bohr does not teach or suggest "a backside via of the integrated circuit". The integrated circuit chip 100 of FIGS. 1 and 2 of Applicant's admitted prior art does not disclose a backside via. FIG. 15 of Bohr does not disclose an integrated circuit comprising a backside via; i.e., the backside via in FIG. 15 is not disclosed by Bohr as being comprised by an integrated circuit. . Thus, the Examiner has not cited any prior art that discloses "a backside via of the integrated circuit" as required by claim 11.

Furthermore, Applicant respectfully contends that the Examiner's argument for modifying Applicant's admitted prior art with the alleged teaching of Bohr is not persuasive. The Examiner argues that "it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die to a substrate (column 12, lines 35-37)."

In response, Applicant contends that FIG. 1 of Applicant's admitted prior art discloses front-side solder balls 155 which are adapted to electrically and mechanically couple the integrated circuit chip 100 to a substrate (such as to a chip carrier or circuit board as is well known in the art). The Examiner has not disclosed any motivation in the prior art for coupling the integrated circuit chip 100 to a substrate at the backside of the integrated circuit chip 100. Thus, it is not obvious to incur extra structural complexity, additional fabrication steps, and additional cost to add a capability that already is available to the integrated circuit chip 100 of FIG. 1 of Applicant's admitted prior art.

Moreover, Applicant's admitted prior art teaches away from use of a backside via to connect the pins 175 in FIG. 1 of Applicant's admitted prior art to a substrate through a backside via. See specification, Paragraph 6, which recites: "There is no wiring in portions of M1 level 120 and M2 level 125 contained within redistribution portion 170. A plurality of core I/O pins 175 are located in redistribution portion 170 at M3 level 130". In other words, FIG. 1 shows that a backside via or other conductive wiring would have to located in the redistribution portion 170 in order for the I/O pins 175 to be connected to a substrate through the backside of the integrated circuit chip 100. However, the preceding quote from the specification teaches away from placing such conductive wiring in the redistribution portion 170.

Based on the preceding arguments, Applicants respectfully maintain that claim 11 is not unpatentable over Bohr, and that claim 11 is in condition for allowance. Since claims 12 and 15-16 depend from claim 11, Applicants contend that claims 12 and 15-16 are likewise in condition for allowance.

In addition with respect to claim 12, Applicant disagrees with the Examiner's allegation

that Applicant's admitted prior art discloses "additional I/O pins contained in metallization layer (145)", since the only I/O pins disclosed in FIG. 1 and the specification are the I/O pins 175 identified by the Examiner in relation to claim 11.

In addition with respect to claim 15, Applicant disagrees with the Examiner's allegation that Applicant's admitted prior art discloses "additional predefined circuitry having a plurality of I/O pins contained in metallization layer (140)", since the only I/O pins disclosed in FIG. 1 and the specification are the I/O pins 175 identified by the Examiner in relation to claim 11.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

Date: 12/15/2004

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